LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-17 (Cancelled)

18. (Currently Amended) A power estimation system, comprising:

means for determining switching power related parameters by evaluating predetermined characterizations that functionally relate a first set of circuit design characteristics as a function of switching power related parameters, the means for determining switching power related parameters comprising means for determining crossover current over a plurality of channel connected regions by evaluating predetermined crossover equations with respective crossover current parameters for a given channel connected region over a plurality of channel connected regions, and summing the determined crossover currents to generate a total crossover current;

means for determining leakage power related parameters by evaluating predetermined characterizations that functionally relate a second set of circuit design characteristics as a function of leakage power related parameters; and

means for generating a total power estimate based on the switching power related parameters and the leakage power related parameters.

19. (Currently Amended) The system of claim 18, the means for determining switching power related parameters comprising ~~means for determining crossover current and~~ means for determining switching capacitance.

20. (Original) The system of claim 18, the means for determining leakage power related parameters comprising means for determining gate tunneling leakage and means for determining source-to-drain leakage.

21. (Original) A power estimation method for a circuit design, comprising:

computing at least one switching power related parameter based on a first set of circuit design characteristics and a first predetermined characterization of switching power related parameters as a function of the first set of circuit design characteristics;

computing at least one leakage power related parameter based on a second set of circuit design characteristics and a predetermined characterization of leakage power related parameters as a function of the second set of circuit design characteristics, the computing at least one leakage power related parameter comprising determining gate tunneling leakage by adding a sum of transistor gate areas of p-type devices multiplied by a predetermined p-type leakage coefficient to a sum of transistor gate areas of n-type devices multiplied by a predetermined n-type leakage coefficient, and determining source-to-drain leakage by adding a sum of transistor gate areas of high voltage threshold (HVT)-type devices multiplied by a predetermined HVT-type leakage coefficient to a sum of transistor gate areas of low voltage threshold (LVT)-type devices multiplied by a predetermined LVT-type leakage coefficient; and

determining total circuit design power based on the computed at least one switching power related parameter and the computed at least one leakage power related parameter.

22. (Original) The method of claim 21, the computing at least one switching power related parameter comprising determining switching capacitance by multiplying node capacitance by an associated predetermined activity factor for a plurality of nodes, and summing the switching capacitances to generate a total switching capacitance, and determining crossover current by evaluating predetermined equations that functional relate channel connected region characteristics to crossover current, and summing crossover current over a plurality of channel connected regions.

23. (Cancelled)

24. (Currently Amended) A computer-readable medium having computer-executable instructions for performing the method of claim ~~23~~ 21.

25. (Original) The method of claim 21, further comprising:

executing an analysis tool for a plurality of circuit design instances;

computing a plurality of power estimates associated with the plurality of circuit design instances; and

comparing the power estimates to determine an optimal circuit design.

26. (Currently Amended) The system of claim 19, wherein the means for determining switching capacitance determines switching node capacitance over a plurality of nodes by multiplying node capacitance by a predetermined activity factor associated with a given node over a plurality of nodes, and summing the determined switching capacitances to generate a total switching capacitance~~, and the means for determining crossover current determines crossover currents over a plurality of channel connected regions by evaluating predetermined crossover equations with respective crossover current parameters for a given channel connected region over a plurality of channel connected regions, and summing the determined crossover currents to generate a total crossover current~~.

27. (Currently Amended) The system of claim ~~26~~ 18, the means for determining leakage power related parameters determines leakage currents for a plurality of transistor devices by multiplying predetermined leakage coefficients associated with a given transistor type by the sums of transistor gate areas associated with the given type for a plurality of transistor types, and summing the determined leakage currents to generate a total leakage current.

28. (Currently Amended) The system of claim ~~27~~ 18, the means for generating a total power estimate determines the total circuit power associated with the circuit design by evaluating the equation:

$$P_{TOTAL} = C_{SWITCHING} * V_{SUPPLY}^2 * f + I_{CROSSOVER} * V_{SUPPLY} + I_{LEAKAGE} * V_{SUPPLY}$$

where $C_{SWITCHING}$ is ~~the~~ a total switching capacitance of the circuit design, V_{SUPPLY} is the supply voltage of the circuit design, f is the frequency of the clock of the circuit design, $I_{CROSSOVER}$ is ~~the~~ a total crossover current of the circuit design and $I_{LEAKAGE}$ is ~~the~~ a total leakage current of the circuit design.

29. (Previously Presented) The method of claim 22, wherein the crossover current characteristics comprise transistor device gate widths, input voltage slopes and capacitive load information associated with the plurality of channel connected regions.

30. (New) A power estimation system, comprising:

means for determining switching power related parameters by evaluating predetermined characterizations that functionally relate a first set of circuit design characteristics as a function of switching power related parameters;

means for determining leakage power related parameters by evaluating predetermined characterizations that functionally relate a second set of circuit design characteristics as a function of leakage power related parameters, the means for determining leakage power determines leakage currents for a plurality of transistor devices by multiplying predetermined leakage coefficients associated with a given transistor type by the sums of transistor gate areas associated with the given type for a plurality of transistor types, and summing the determined leakage currents to generate a total leakage current; and

means for generating a total power estimate based on the switching power related parameters and the leakage power related parameters.

31. (New) The system of claim 30, the means for determining leakage power related parameters comprising means for determining gate tunneling leakage and means for determining source-to-drain leakage.

32. (New) The system of claim 30, the means for determining switching power related parameters comprising means for determining switching capacitance over a plurality of nodes by multiplying node capacitance by a predetermined activity factor associated with a given node over a plurality of nodes, and summing the determined switching capacitances to generate a total switching capacitance, and means for determining crossover current over a plurality of channel connected regions by evaluating predetermined crossover equations with respective crossover

current parameters for a given channel connected region over a plurality of channel connected regions, and summing the determined crossover currents to generate a total crossover current.

33. (New) A power estimation method for a circuit design, comprising:

analyzing the circuit design to determine a switching capacitance characterization, a crossover current characterization and a leakage current characterization associated with the circuit design;

storing the switching capacitance power characterization, the crossover current characterization and the leakage current characterization;

receiving a plurality of circuit design characteristics associated with a given instance of the circuit design;

computing total switching capacitance based on node capacitance of the given instance of the circuit design and the switching capacitance characterization;

computing total crossover current based on crossover current parameters of the given instance of the circuit design and the crossover current characterization;

computing total leakage current based on transistor gate area of the given instance of the circuit design and the leakage current characterization; and

determining total power of the given instance of the circuit design based on the computed total switching capacitance, total crossover current and total leakage current.

34. (New) The method of claim 33, the crossover current characterization comprises predetermined crossover current equations that functional relate channel connected region characteristics to crossover current.

35. (New) The method of claim 34, wherein the total crossover current is computed by evaluating predetermined crossover equations with respective crossover current parameters for a given channel connected region over a plurality of channel connected regions, and summing the determined crossover currents to generate the total crossover current.

36. (New) The method of claim 33, the switching capacitance characterization comprises a predetermined activity factor associated with a given node over a plurality of nodes.

37. (New) The method of claim 36, wherein the total switching capacitance is determined by multiplying node capacitance by a predetermined activity factor associated with a given node over a plurality of nodes, and summing the determined switching capacitances to generate the total switching capacitance.

38. (New) The method of claim 33, the leakage current characterization comprises at least one predetermined leakage coefficient associated with at least one given transistor type.

39. (New) The method of claim 38, wherein a total leakage current is computed by multiplying a predetermined leakage coefficient associated with a given transistor type by the sums of transistor gate areas associated with the given type for at least one transistor type, and summing the determined leakage currents to generate the total leakage current

40. (New) A computer-readable medium having computer-executable instructions for performing the method of claim 33.

41. (New) The method of claim 33, further comprising:

executing an analysis tool for a plurality of circuit design instances;

computing a plurality of power estimates associated with the plurality of circuit design instances; and

comparing the power estimates to determine an optimal circuit design.

42. (New) The method of claim 33, wherein the determining total power of the given instance of the circuit design is based on evaluating the equation:

$P_{TOTAL} = C_{SWITCHING} * V_{SUPPLY}^2 * f + I_{CROSSOVER} * V_{SUPPLY} + I_{LEAKAGE} * V_{SUPPLY}$

where $C_{SWITCHING}$ is a total switching capacitance of the circuit design instance, V_{SUPPLY} is the supply voltage of the circuit design instance, f is the frequency of the clock of the circuit

design instance, $I_{CROSSOVER}$ is a total crossover current of the circuit design instance and $I_{LEAKAGE}$ is a total leakage current of the circuit design instance.